



Bridging The Gap Between Education and Industry

Training programs for Professionals & Engineering (Diploma, Graduate & PG) students.

Faculty Training Programs for Engineering Institutions.

Vocational Training for Students and School dropouts of below 10th or 10th/12th class.

Enabling Training to all in Non-formal Education Sector.

Diploma Programs in VLSI

Conduction of Training under aegis of Scientechnologies Pvt. Ltd., An ISO 9001:2000 Certified Company
Manufacturer of Test & Measurement Instruments, Technology Trainers & Software as well.

*Make a career
in
VLSI*

- Flexible Program
- Full Time and Part Time
- Faculty Training Program
- Industrial Projects
- Placement Support

The Program is emphasis on the development of important graduate qualities such as life long learning and problem solving in the field of digital design. Students start working on the practical projects / problems right from the beginning of the course. Project handouts assists student to learn the software tools & design techniques through step by step approach during the course.

This project based learning approach has yielded high student satisfaction & achievements.

Standard VLSI Program

4 Months, Seven Modules, Full Time, Mini and Major Projects, Certificate and Grade Sheet

<p>Modules :</p> <p>Module1 : Introduction to VLSI Design Analog & Digital Design 1 Weeks</p> <p>Module2 : Introduction to Verilog HDL Xilinx & Altera Tool Study 3 Weeks</p> <p>Module3 : Introduction to VHDL Xilinx & Altera Tool Study 3 Weeks</p> <p>Module4 : Advance HDL 1 Weeks</p> <p>Module5 : CPLD Architecture , Mini Project & Applications 1 Weeks</p> <p>Module6 : FPGA Architecture, Introduction to DSP, Mini Project & Applications 1 Weeks</p> <p>Module7 : Board Design issues, Project & Seminar 6 Weeks</p>	<p>Module 1 (Introduction to VLSI & Analog-Digital Design)</p> <p>Description : Fast track module for Analog, Digital Electronics, Introduction to VLSI etc. Which will help students during there design work.</p> <p>Duration : 1 Week</p> <p>Level - Good fundamentals</p> <p>Who Should Attend ? : Engineers who want to design digital System.</p> <p>Prerequisites : Basic Knowledge of Analog and Digital Electronics</p> <p>After Completing this module : Engineer will be in a position to design an Analog and Digital System.</p> <p>Module Outline :</p> <ul style="list-style-type: none"> ➤ Introduction to IC ➤ History of IC Design ➤ IC Complexity ➤ What is VLSI ➤ EDA Tools ➤ VLSI Terminologies ➤ Fast Track Analog Design Simulation ➤ Fast Track Digital Design Simulation <p>LabWork : Digital Analog circuit design using TINA Pro simulation tool</p>
<p>Module 2 (Introduction to Verilog HDL, Xilinx ISE and Altera quartus Tool)</p> <p>Description : This comprehensive module is a thorough introduction to the Verilog language. The Emphasis is on writing RTL source code. Target device is from Xilinx & Altera. The information gained can be applied to any Digital Design by using a top-down synthesis design approach. In this module, you will gain valuable hands-on experience.</p> <p>Duration : 3 Weeks</p> <p>Level : Fundamentals</p> <p>Who Should Attend ? : Engineers who want to use Verilog HDL effectively for modeling, design and synthesis of Digital design</p> <p>Prerequisites : Basic Digital Design Knowledge</p> <p>After Completing this module : You will be ready to design any digital design using Verilog HDL.</p> <p>Module Outline :</p> <ul style="list-style-type: none"> ➤ Basic Language Elements ➤ Module, Port Connection Rules ➤ Levels of Abstraction ➤ Task and Functions ➤ Procedural continuous Assignment ➤ Users Define Primitives. ➤ Switch level Modeling <p>LabWork : The Labs for this Module provides a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the Labs. The labs are written, synthesized, simulated and implemented by the student. Student will simulate some good applications</p>	<p>Module 3 (Introduction to VHDL, XILINX ISE & Altera Quartus Tool)</p> <p>Description : This comprehensive module is a thorough introduction to the VHDL language, learn about ISE quartus tool. The Emphasis is on writing RTL source code. Target device is from Xilinx & Altera. The information gained can be applied to any digital Design by using a top-down synthesis design approach. In this module, you will gain valuable hands-on experience.</p> <p>Duration : 3 Weeks</p> <p>Level : Fundamentals</p> <p>Who Should Attend ? : Engineers who want to use VHDL effectively for modeling, design and synthesis of Digital design</p> <p>Prerequisites : Basic Digital Design Knowledge</p> <p>After Completing this module : You will be ready to design any digital design using VHDL.</p> <p>Module Outline :</p> <ul style="list-style-type: none"> ➤ Basic Language Elements ➤ Level of abstraction ➤ Entity and Architecture ➤ Process and Procedure ➤ Functions and Subprogram ➤ Configuration, Package ➤ Attribute and Generic <p>LabWork : The Labs for this Module provides a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the Labs. The labs are written, synthesized, simulated and implemented by the student. Student will simulate some good applications</p>
<p>Module 4 (Advanced HDL)</p> <p>Description : This comprehensive module is a thorough introduction to the Advanced VHDL language. The emphasis is on writing the state machine, Pipelined Architecture, Memories, Control and Data path issues etc. The information gained can be applied to any Advanced design by using a Top-down synthesis design approach</p> <p>Duration : 1 Week</p> <p>Level : strong in digital design</p> <p>Who Should Attend ? : Digital designers who use xilinx & Altera software extensively and who need to learn the Advanced Digital design</p> <p>Prerequisites : Thorough in HDL Languages (VHDL / Verilog HDL), Digital Design experience</p> <p>After Completing this module : You will be ready to design any digital design using HDL.</p> <p>Module Outline :</p> <ul style="list-style-type: none"> ➤ State Machine Analysis and Design ➤ Pipelined Architecture ➤ Memories (RAM, ROM, FIFO) ➤ Control and Datapath issues <p>LabWork : The Labs for this Module provides a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the Labs. The labs are written, synthesized, simulated and implemented by the student. Student will simulate some good applications</p>	<p>Module 5 (CPLD Architecture, Application and Mini Project)</p> <p>Description This module provides you with an introduction to design with Xilinx CPLD by using the ISE software tools. You will learn the basics of ISE software flow, how to interpret CPLD report for optimized performance design, physical implementation and testing on CPLD development platform.</p> <p>Duration : 1 Week</p> <p>Level : Fundamentals</p> <p>Who Should Attend ? : Digital designers who have working knowledge of basic HDL and who are new to Xilinx CPLD</p> <p>Prerequisites : Basic HDL Knowledge (VHDL / Verilog HDL), Digital Design experience</p> <p>After Completing this module :</p> <ul style="list-style-type: none"> ➤ Architecture of CPLD ➤ CPLD Design Flow. ➤ Timing constraints and Pin Assignment. ➤ Board Level Implementation <p>Module Outline :</p> <ul style="list-style-type: none"> ➤ PAL issues ➤ PLD issues ➤ CPLD issues ➤ CPLD Architecture ➤ CPLD Design flow ➤ CPLD Applications ➤ CPLD based Mini Projects <p>LabWork :</p> <ul style="list-style-type: none"> ➤ Xilinx CPLD flow ➤ Constraint for CPLD
<p>Module 6 (FPGA Architecture, Application and Mini Project)</p> <p>Description : This module provides you with an introduction to design with Xilinx FPGA by using the ISE software tools. You will learn the basics of ISE software flow, how to interpret FPGA report for optimized performance design, physical implementation and testing on FPGA development platform.</p> <p>Duration - 1 Week</p> <p>Level - Fundamentals</p> <p>Who Should Attend ? : Digital designers who have working knowledge of basic HDL and who are new to Xilinx FPGA</p> <p>Prerequisites : Basic HDL Knowledge (VHDL / Verilog HDL), Digital Design experience</p> <p>After Completing this module :</p> <ul style="list-style-type: none"> ➤ Architecture of FPGA ➤ FPGA Design Flow. ➤ Timing constraints and Pin Assignment. ➤ Board Level Implementation <p>Module Outline :</p> <ul style="list-style-type: none"> ➤ PAL issues ➤ PGA issues ➤ FPGA issues ➤ FPGA Architecture ➤ FPGA Design flow ➤ FPGA Applications ➤ FPGA based Mini Projects <p>LabWork :</p> <ul style="list-style-type: none"> ➤ Xilinx FPGA flow ➤ Constraint for FPGA 	<p>Module 7 (Seminar and Live Projects)</p> <p>Description : This module provides Highest Level of design</p> <p>Duration : 6 Weeks</p> <p>Level : Expertise in Digital Design</p> <p>Who Should Attend ? : One who had gone through all the previous modules or having prior knowledge of all the above modules.</p> <p>Prerequisites : Sound knowledge of in Digital Design, HDL Language & Xilinx design flow</p> <p>After Completing this module : Student will understand the Industrial VLSI Project cycle and how to work in a team.</p> <p>Module Outline :</p> <ul style="list-style-type: none"> ➤ Specifications Study ➤ Bill of Material ➤ Writing HDL Code (Verilog / VHDL) ➤ Synthesis ➤ Implementation ➤ Verification ➤ Prototype testing ➤ Board design issues <p>LabWork :</p> <ul style="list-style-type: none"> ➤ Major Project ➤ Seminars

Basic VLSI Program

1 Month, 4 Modules, Full Time, Mini Projects, Certificate

VLSI Fundamental and Digital Design :

Digital Electronics, Introduction to VLSI etc.

- Introduction to IC, History of IC Design, IC Complexity
- What is VLSI ?
- EDA Tools
- VLSI Terminologies
- Fast Track Digital Design Simulation

Introduction to Verilog HDL or VHDL :

This comprehensive module is a thorough introduction to the Verilog HDL and VHDL language. The Emphasis is on writing RTL source code. Target device is from Xilinx & Altera.

- | | |
|------------------------------------|--------------------------------|
| ➤ Basic Verilog Language Elements | ➤ Basic VHDL Language Elements |
| ➤ Module, Port Connection Rules | ➤ Level of abstraction |
| ➤ Levels of Abstraction | ➤ Entity and Architecture |
| ➤ Task and Functions | ➤ Process and Procedure |
| ➤ Procedural continuous Assignment | ➤ Functions and Subprogram |
| ➤ Users Define Primitives. | ➤ Configuration, Package |
| ➤ Switch level Modeling | ➤ Attribute and Generic |

FPGA Architecture, Application and Mini Project

This module provides you with an introduction to design with Xilinx CPLD & FPGA by using the ISE software tools.

- PAL issues
- PLD & PGA issues
- CPLD & FPGA issues
- CPLD & FPGA Architecture
- CPLD & FPGA Design flow
- CPLD & FPGA Applications

Mini Projects based on FPGA and CPLD

- Xilinx CPLD & FPGA Flow
- Constraint for CPLD & FPGA

Part Time VLSI Program

1 Month, 4 Modules, Part Time, Lab Work, Certificate

VLSI Fundamental and Digital Design

Digital Electronics, Introduction to VLSI etc. Which will help students during there design work.

- Introduction to IC, History of IC Design, IC Complexity
- What is VLSI ?
- EDA Tools
- VLSI Terminologies
- Fast Track Digital Design Simulation

Introduction to Verilog HDL or VHDL-

This comprehensive module is a thorough introduction to the Verilog HDL and VHDL language. The Emphasis is on writing RTL source code. Target device is from Xilinx.

- | | |
|------------------------------------|----------------------------|
| ➤ Basic Language Elements | ➤ Basic Language Elements |
| ➤ Module, Port Connection Rules | ➤ Level of abstraction |
| ➤ Levels of Abstraction | ➤ Entity and Architecture |
| ➤ Task and Functions | ➤ Process and Procedure |
| ➤ Procedural continuous Assignment | ➤ Functions and Subprogram |
| ➤ Users Define Primitives. | ➤ Configuration, Package |
| ➤ Switch level Modeling | ➤ Attribute and Generic |

FPGA Architecture, Application and Mini Project

This module provides you with an introduction to design with Xilinx CPLD & FPGA by using the ISE software tools.

- PAL issues
- PLD & PGA issues
- CPLD & FPGA issues
- CPLD & FPGA Architecture
- CPLD & FPGA Design Flow
- CPLD & FPGA Applications

Lab Work based on FPGA and CPLD

- Xilinx CPLD & FPGA Flow
- Constraint for CPLD & FPGA

Faculty VLSI Program

7 Days, Full Time, Tool Specific Training

- Digital Electronics Design, Introduction to VLSI Design & Applications
- Introduction to Verilog HDL or VHDL
- Xilinx ISE Tool Study Complete Flow and Lab Work
- Altera Quartus Tool Study, Complete Flow and Lab Work
- CPLD Architecture & Applications
- FPGA Architecture & Applications
- Project Guideline and Hands on Practice

Note - Student can also enroll for selected Module of Standard VLSI Program



Training Hall

Library

Resources

- A well furnished Seminar Hall having capacity of more than 50 Students.
- Individual systems are provided for the students.
- New concept of study by combining theoretical and practical classes.
- Hard copy of study material for quick reference.
- Inter modular exams test
- Multiple copies of basic to Advanced books from various Publications.
- Datasheets of Xilinx, Altera, Philips Analog Devices etc.
- Software CD
- Library & Lab facility
- CPLD and FPGA Development Platforms
- Test and Measurement Instruments (Logic Analyzer, DSO, CRO, Function Generator, Multi Lab etc.) provided during Labwork and Projects.
- Easy availability of Electronic Components during projects.
- Canteen Facility



Eligibility

BE / B.Tech / M.Tech / Equivalent degree in ECE, EEE, CSE students (Including Third & Final Year).

Selection Criteria

Based on the performance of entrance test followed by interview.

Examination Format

Test will be conducted in Basic Digital Design hardware design, Microprocessor, Microcontroller and new Trends in Electronics. The test paper consists of objective, short answer & problem solving type and Design based questions.



We also conduct Vocational Training for Serving, Ex-servicemen & Retiring Armed Forces Personnel

For detailed Calendar of courses and registration Please contact :

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94-101, Electronic Complex, Pardesipura, Indore - 452 010 India, Tel : +91-731-2570301/02, 2556638, Fax : 731-2555643, E-mail : info@scientech.bz, Website : www.scientech.bz